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In the Claims:

1-38. (Cancelled)

39. (Currently Amended) A semiconductor device comprising:

an insulator layer;

a planar transistor formed on a first portion of a semiconductor layer, the first portion of the semiconductor layer overlying the insulator layer, and the first portion of the semiconductor layer having a first thickness;

a multiple-gate transistor formed on a second portion of the semiconductor layer, the second portion of the semiconductor layer overlying the insulator layer, the second portion of the semiconductor layer having a second thickness, and the second thickness being larger than the first thickness; and

the planar transistor comprising:

a planar channel formed from the first portion of the semiconductor layer;

a gate dielectric having vertical portions on opposite sidewalls of the planar channel and a horizontal portion on a top surface of the planar channel;

a gate electrode overlying the gate dielectric, wherein the gate electrode has vertical portions on the vertical portions of the gate dielectric and a horizontal portion on the horizontal portion of the gate dielectric; and

source and drain regions formed in the second <u>first</u> portion of the semiconductor layer oppositely adjacent the gate electrode.

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- 40. (New) The semiconductor device of claim 39, wherein the first thickness is less than about a half of a gate length of the planar transistor.
- 41. (New) The semiconductor device of claim 40, wherein the first thickness is less than about one-third of a gate length of the planar transistor.
- 42. (New) The semiconductor device of claim 39, wherein the first thickness is less than about 400 angstroms.
- 43. (New) The semiconductor device of claim 39, wherein the second thickness is greater than about 100 angstroms.
- 44. (New) The semiconductor device of claim 39, wherein the gate dielectric of the planar transistor comprises a material selected from a group consisting of silicon oxide, silicon oxynitride, high-k dielectric material, a dielectric with a relative permittivity larger than about 5, and combinations thereof.
- 45. (New) The semiconductor device of claim 39, wherein the gate electrode of the planar transistor comprises a material selected from a group consisting of a metal, a metallic nitride, a metallic silicide, poly-crystalline silicon, and combinations thereof.
- 46. (New) The semiconductor device of claim 39, wherein a gate dielectric of the multiplegate transistor comprises a material selected from a group consisting of silicon oxide, silicon

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oxynitride, high-k dielectric material, a dielectric with a relative permittivity larger than about 5, and combinations thereof.

- 47. (New) The semiconductor device of claim 39, wherein a gate electrode of the multiple-gate transistor comprises a material selected from a group consisting of a metal, a metallic nitride, a metallic silicide, poly-crystalline silicon, and combinations thereof.
- 48. (New) The semiconductor device of claim 39, wherein corners of the semiconductor layer are rounded at edges of active regions of the planar and multiple-gate transistors.